ECE3081: Digital System Design with FPGAs

Programme: B.Tech. (ECE) Year: 3rd Semester: 2nd
Course:Program Elective (ECE, CCE) Credits: 3 Hours: 40

Course Context and Overview (100 words): The goal of the course is to introduce digital design techniques using field programmable gate arrays (FPGAs). We will discuss FPGA architecture, digital design flow using FPGAs, and other technologies associated with field programmable gate arrays.

Prerequisites Courses: Digital Circuits and Systems

Course outcomes(COs):

On completion of this course, the students will have the ability to:	
CO1:	Analyze the results of logic and timing simulations and to use these simulation results to debug digital system.
CO2:	Develop skills, techniques and learn state-of-the-art engineering tools to design, implement and test modern-day digital systems on FPGAs.
CO3:	Learn by using Xilinx Foundation tools and Hardware Description Language (VHDL).
CO4:	Understand modern CAD tools for FPGA design.
CO5:	Learn through hands-on experimentation the Xilinx tools for FPGA design as well as the basics of VHDL to design and simulate systems.

Course Topics:

Topics	Lecture Hours	
UNIT - I **1. Fundamental Concepts**	4	
1.1 Introduction, FPGA's History and Future, The key thing about FPGAs	2	4
1.2 Fusible link technologies, Antifuse technologies, Mask-programmed devices, PROMs,	1	
1.3 EPROM-based technologies, EEPROM-based technologies, FLASH-based technologies, SRAM-based technologies	1	
UNIT - II **2. Programmable Logic to ASICs**	4	4
2.1 Programmable Read Only Memories (PROMs)	1	
2.2 Programmable Logic Arrays (PLAs), Programmable Array Logic (PALs)	1	
2.3 The Masked Gate Array ASIC, CPLDs and FPGAs.	2	
UNIT - III **3. Complex Programmable Logic Devices (CPLDs)**	6	6
3.1 CPLD Architectures, Function Blocks, I/O Blocks	2	
3.2 Clock Drivers, Interconnect	1	
3.3 CPLD Technology and Programmable Elements	2	

3.4 Embedded Devices, Summary: CPLD Selection Criteria	1	
UNIT - IV **4. Field Programmable Gate Arrays (FPGAs)**	6	6
4.1 FPGA Architectures, Configurable Logic Blocks	2	
4.2 Configurable I/O Blocks, Embedded Devices, Programmable Interconnect	2	
4.3 Clock Circuitry, SRAM vs. Antifuse Programming	2	
UNIT - V **5. Alternative FPGA Architectures**	8	8
5.1 Antifuse versus SRAM, Fine-medium and coarse grained architectures, MUX vs. LUT based-logic blocks	2	
5.2 CLBs versus LABs slices, Fast Carry Chains, Embedded RAMs	2	
5.3 Embedded multipliers, adders, MACs	2	
5.4 Embedded processor cores (hard and soft), Clock trees and clock managers, General Purpose I/O	2	
UNIT - VI **6. VHDL**	12	12
6.1 Introduction	1	
6.2 Behavioral, Data Flow, Structural Models	3	
6.3 Simulation Cycles, Concurrent Statements, Sequential Statements	2	
6.4 Delay Models, Sequential Circuits, FSM coding	2	
6.5 Test bench	2	

Textbook references (IEEE format):

Reference books:

[1]. Navabi, Zinalabedin. *"VHDL: Analysis and Modeling of Digital Systems"*, 2nd. ed. 1998. McGraw Hill. ISBN 0-07-046479-0

[2]. J. Armstrong and F. G. Gray, *"VHDL Design: Representation and Synthesis"* 2nd Edition, 2000

[3]. Edward McCluskey, *"Logic Design Principles"* Prentice Hall, 1986

[4]. Pak Chan et. al. *"Digital Design Using FPGAs"* Prentice Hall, 1994

[5]. Kevin Skahill, *"VHDL for Programmable Logic"*, Cypress SemiConductor.

[6]. Jesse H. Jenkins, *"Designing with FPGAs and CPLDs"* Prentice Hall, 1994

Evaluation Methods:

Item	Weightage
Quiz, Assignments	20
Midterm	30
Final Examination	50

Prepared By:

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