Programme: B. Tech. (CSE)	Course Title: Computer Organization and Architecture			Course Code: CSE216
Type of Course: Program Core	Prerequisites: Basic Electronics			Total Contact Hours: 40 Theory + 20 Lab
Year/Semester: 2/Odd	Lecture Hrs/Week: 3	Tutorial Hrs/Week: 0	Practical Hrs/Week: 2	Credits: 4

Learning Objective:

The course aims to provide a basic understanding of a digital computer. The course will familiarize students with the von Neumann architecture. Functioning of processors, trends and issues in modern processors will be discussed (pipelining, performance etc.). The course will cover memory hierarchy including cache and virtual memory. Different ways of communicating with I/O devices and concept of bus system within the computer will be studied. The course will also discuss the design of an instruction set and how instructions are executed, along with identifying different addressing modes.

Course outcomes (COs):

On completion of this course, the students will have the ability to:		Bloom's Level
CO-1	Describe the organization of a typical computer and internal representation of data	**1**
CO-2	Design processor architecture including data-path, control-unit and instruction set	**2**
CO-3	Explain instruction level parallelism	**1, 2**
CO-4	Describe and demonstrate memory hierarchy	**3**
CO-5	Describe interfacing and communication mechanisms with I/O devices and functional units	**3, 4**

Course Topics	Lecture Hours	
UNIT – I (Introduction:)		**4**
1.1 Introduction to computers	**1**	
1.2 Data representation and arithmetic.	**2**	
1.3 RISC/CISC, Superscalar architecture, Array and vector processors, Multiprocessors, Multicomputers, advanced processors, Flynn taxonomy	**1**	
UNIT – II (Instruction Set Architecture:)		
1.1 Memory models, Registers	**1**	
1.2 Instruction types	**1**	
1.3 Instruction formats	**1**	

1.4 Addressing modes	**1**	9
1.5 Expanding opcodes	**1**	
1.6 Flow of control: Sequential, Branching, Co-routines, Traps, Interrupts	**2**	
Assembly language		
2.1 Introduction to assembly language, pseudoinstructions, macros	**1**	
2.2 Assemblers, Symbol Table, Linkers, Loaders	**1**	
UNIT – III (Central Processing Unit:)		**11**
1.1 Instruction execution cycle	**1**	
1.2 Data Path	**1**	
1.3 Control Unit: hardwired, microprogrammed	**4**	
1.4 Performance, benchmarks	**1**	
Pipelining		
2.1 Pipelines: hazards, branch prediction, speculative execution, out of order execution	**4**	
UNIT-IV (Memory system)		**10**
1.1 Storage systems: Magnetic disks, CDs, Blu-Ray, RAID; Memory hierarchy	**1**	
1.2 SRAM, DRAM, address translation	**2**	
1.3 Cache memory: principle of locality, main memory to cache mapping, cache coherence	**3**	
1.4 Virtual memory: Paging, page replacement, segmentation, fragmentation, TLB	**3**	
1.5 Memory and cache performance metrics	**1**	
UNIT-V (Bus System)		**6**
1.1 Bus width, bus clocking	**1**	
1.2 Bus arbitration	**1**	
1.3 Bus operations	**1**	
I/O interfacing:		
2.1 Handshaking, buffering, programmed I/O, interrupt driven I/O	**1**	
2.2 Interrupt structures: vectorized, prioiritized, interrupt acknowledgment	**1**	
2.3 Interrupt handling, DMA	**1**	

List of experiments:

Experiment No.	Topic
0	Tools discussion: MARS, TKGATE
1	Assembly Language Programming 1:- Basic Programming (Using MARS)
2	Assembly Language Programming 2:- Iterative programming (Using MARS)
3	Assembly Language Programming 3:- Subroutine programming (Using MARS)
4	Basic circuit design (Adder, Subtractor, Basic ALU) (Using TKGATE)
5	Memory design and Data Access (Using TKGATE)
6	ISA Design and CPU simulation-1 (Using TKGATE)
7	ISA Design and CPU simulation-2 (Using TKGATE)
8	Simulation of pipeline execution (RWR, WAW, WAR, RAW)
9	Simulation of Memory Mapping

Textbook References:
Text Book:

Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Naraig Manjikian, Computer Organization, 6th ed. McGraw Hill, 2012

Reference books:

A.S. Tanenbaum, *Structured Computer Organization,* 5th ed. Prentice Hall, 2005.
D.A. Patterson and J.L. Hennessy, *Computer Architecture: Hardware/Software Interface*, 4th ed. Morgan Kaufmann, 2011.

Evaluation Method	
Item	**Weightage (%)**
Quizzes/Assignments	25% (Two Quizzes 10 and 15)
Midterm	20%
Endterm	30%
LAB	
Component	**Weightage**
Continuous evaluation	0.25 for each assignment - For 6 assignments 7.5 Lab quiz- Assembly language programming 6 Programming quiz/assignment in C Plagiarism will be checked. In case similarity >20%, zero marks will be awarded for the assignment. No request will be entertained in this regard.
Project	10%

*Please note, as per the existing institute's attendance policy the student should have a minimum of 75% attendance. Students who fail to attend a minimum of 75% lectures will be debarred from the End Term/Final/Comprehensive examination.

CO and PO Correlation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3		2		3								2	2	1
CO2	3	3	2		1							1	2	2	1
CO3	3	3	2									1	2	2	1
CO4	3	3	2									1	2	2	1
CO5	3	3	2									1	2	2	1

Last Updated On: August 10, 2021

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Approved By: