

Programme: M. Tech. (ECE)	Course Title: VLSI Circuits & Systems			Course Code:
Type of Course: Core	Prerequisites: NIL			Total Contact Hours: 40
Year/Semester:	Lecture	Tutorial Hrs/Week	Practical Hrs/Week	Credits 4

Learning Objective:

The objective of this course is to present the field of VLSI in its entirety. VLSI deals with conception, design and manufacture of complex integrated circuits. This course will make students aware of the fundamentals of any chip fabrication and challenges faced by IC designers at circuit level as well at system level. Topics to be covered include overview of VLSI, silicon processing, CMOS logic, circuit design fundamentals, chip design flow etc. The course also introduces basics of Verilog HDL programming and circuit design through industry specific CAD tool.

Course outcomes (COs):

On completion of this course, the students will have the ability to:		Bloom's Level
CO-1	Recognize importance of CMOS in VLSI, understand and apply CMOS logic in realization of complex gate	1, 2, 3
CO-2	Understand silicon processing and CMOS process flow	2
CO-3	Simplify and analyze complex circuits	4
CO-4	Recognize low power design solutions	1
CO-5	Understand physical design at system level	2
CO-6	Understand and analyze wireless communication circuits	2, 6

Course Topics:

Topics	Lecture Hours
UNIT – I: VLSI Overview Complexity and Design, General considerations, CMOS Logic, Basic & Complex Logic Design, Transmission gate, clocking and data flow control	7
UNIT – II: Fabrication of CMOS and Layout Silicon Processing, Material Growth, Lithography, CMOS Process flow, Design rule, Cell concepts, Transistor sizing	7
UNIT – III: Circuit Level MOS Transistor physics, current-voltage expression, Small-signal modeling, RC model, CMOS Inverter DC and switching characteristic, Power Dissipation, Transmission Gate and Pass Transistors, Gate Delays, Logical Effort, BiCMOS Drivers, Dynamic CMOS and Dual-Rail Logic circuits	10
UNIT – IV: System Level Chip Design flow, Interconnect Delay model & challenges, Crosstalk & challenges, Interconnect scaling, Floorplanning & Routing, I/O protection circuits, Power	8

Distribution & consumption, Low Power Design considerations	
UNIT – V: Wireless Communication: Circuit Designer Perspective Overview of wireless system, High Speed Amplifier, Low Noise Amplifier, Wideband LNA-DC Bias, Gain, Noise Figure, Narrowband LNA-Impedance Matching, Noise Figure, Power Dissipation, Gain, Design constraints	8

Book References:

Text Books:

- [1] Uyemura John P.: Introduction to VLSI Circuits and Systems, John Wiley and Sons, Edition 2001.
- [2] Sung-Mo (Steve) Kang and Yusuf L: CMOS Digital Integrated Circuits Analysis & Design, TATA McGraw Hill Education, 2002.
- [3] Leung B.: VLSI for Wireless Communication, 2nd Edition Springer, 2011.

Reference book:

- [1] Razavi B.: Design of Analog CMOS Integrated Circuits, Tata McGraw-Hill Edition 2006.
- [2] Weste N. and Harris D.: Principles of CMOS VLSI Design, Addison Wesley. 2004.

Additional Resources:

- www.cmosedu.com
- <http://www.facweb.iitkgp.ac.in/~isg/CAD/>

Evaluation Method:

Item	Weightage (%)
Quizes/Assignments	20
Mid Term	30
End Term	50

* Please note, as per the existing institute’s attendance policy the student should have a minimum of 75% attendance. Students who fail to attend a minimum of 75% lectures will be debarred from the End Term/Final/Comprehensive examination.

CO and PO Correlation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	1						2	1		3	3	1	
CO2	3	3	2						2	1		3	3	1	
CO3	3	3	1						2	1		3	3	1	
CO4	3	2	1						2	1		3	3	1	
CO5	3	3	1						2	1		3	3	1	
CO6	3	3	3	2					2	1		3	3	2	2

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Approved By: