| Programme: B. Tech. (ECE) | Course Title: Digital IC Design | | | Course Code: ECE4082S |
|---|---|---|---|---|
| Type of Course: Program Elective | Prerequisites: Digital Circuits and Systems | | | Total Contact Hours: 40 |
| Year/Semester: 4/Even | Lecture Hrs/Week: 3 | Tutorial Hrs/Week: 0 | Practical Hrs/Week: 0 | Credits: 3 |

**Learning Objective:**

This is a most fundamental Digital Circuit Design course for pursing a major in VLSI. The course introduces the basic concepts of CMOS based IC design. The learning starts with the analysis and design of CMOS inverter. The students will learn delay and power calculations for CMOS circuits as well. The specific materials related to gate sizing, buffering, asymmetric gate, skewed gates, dynamic gates and Domino logic. The course also teaches sequential circuits and feedback. Various flip flop circuits, both static and dynamic are discussed. The course aims to design complex combinational and sequential systems using simple CMOS modules like mirror adder, carry skip adder, carry select adder, square root adder, multipliers – signed and unsigned arithmetic, carry save multipliers.

**Course Outcomes (COs):**

| On completion of this course, the students will have the ability to: | | Bloom's Level |
|---|---|---|
| CO-1 | **Define**, **explain** and **examine** the key delay quantities of a standard CMOS cell | 1, 2, 4 |
| CO-2 | **List** and **evaluate** the power dissipated in a circuit (dynamic and leakage) | 1, 4 |
| CO-3 | **Examine** and **demonstrate** a circuit to perform a certain functionality with specified speed | 3, 4 |
| CO-4 | **Identify** and **solve** the critical path of a combinational or sequential circuit | 2, 3 |
| CO-5 | **Define**, **recognize** and **implement** various combinational systems | 1, 2, 3 |
| CO-6 | **Define** and **implement** various sequential systems | 1, 3 |

| Course Topics | Lecture Hours | |
|---|---|---|
| **Unit-I Fundamentals CMOS inverter** | | |
| **1.1.** The CMOS Inverter construction and Voltage Transfer Characteristics | 3 | 6 |
| **1.2.** Resistance and Capacitance and transient response of CMOS intverte | 3 | |
| | | |
| **Unit –II Power Analysis** | | |
| **2.1.** Dynamic, Short Circuit and Leakage power – Stacking Effect | 3 | 7 |
| **2.2.** Power analysis for Combinational Circuit Design | 2 | |
| **2.3.** Role of capacitance in power calculations. | 2 | |
| | | |
| **Unit-III Delay Analysis** | | |
| **3.1.** Parasitic Delay, Logical Effort and Electrical Effort calculations | 3 | 6 |
| **3.2.** Propagation delay, Contamination delay, Rise time, Fall time, Edge rate. | 3 | |

| | | |
|---|---|---|
| **Unit-IV Gate sizing** | | |
| **4.1.** Gate sizing and Buffering | **2** | **7** |
| **4.2.** Asymmetric gate, Skewed gates, Ratioed logic | **2** | |
| **4.3.** Dynamic Gates and Domino logic and Static Timing Analysis | **3** | |
| | | |
| **Unit –IV Sequential circuits** | | |
| **5.1.** Sequential circuits and feedback. Various D flip flop circuits – Static and Dynamic | **3** | **7** |
| **5.2.** Setup and Hold Time measurement. | **2** | |
| **5.3.** Timing analysis of latch/ flop based systems | **2** | |
| | | |
| **Unit-VI Complex system Design** | | |
| **6.1.** :Adders – Mirror adder, Carry Skip adder, Carry Select adder, Square Root adder | **3** | **7** |
| **6.2.** Multipliers – Signed and Unsigned arithmetic, Carry Save Multiplier implementation | **2** | |
| **6.3.** FSM based systems | **2** | |
| | | |
| **Total Lecture Hours** | **40** | |

## Textbook & References Books

### Text Books:

**[1]** ***Digital Integrated Circuits: A Design Perspective***, Anantha P. Chandrakasan and Jan M. Rabaey, Prentice Hall India Learning Private Limited; 2nd edition

**[2]** ***Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication***, Hubert Kaeslin, Cambridge

### Reference Books:

**[1]** ***Low Power Interconnect Design***, Sandeep Saini, Springer

**[2]** ***Circuits, Devices and Systems***, R.J Smith & R.C Dorf, John Wiley & Sons

### Online sources:

The course will be in sync with the NPTEL course Digital IC Design
https://onlinecourses.nptel.ac.in/noc20_ee05/preview

| Evaluation Method | |
|---|---|
| **Item** | **Weightage (%)** |
| Quizzes and Assignments | **40** |
| Midterm | **20** |
| Final Examination | **40** |

*Please note, as per the existing institute's attendance policy the student should have a minimum of 75% attendance. Students who fail to attend a minimum of 75% lectures will be debarred from the End Term/Final/Comprehensive examination.

**CO and PO Correlation Matrix**

| CO | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 11 | PO 12 | PSO 1 | PSO 2 | PSO 3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | 3 | 3 | 1 | | | | | | 2 | | | 3 | 3 | 1 | |
| CO2 | 3 | 2 | 2 | 1 | | | | | 2 | | | 3 | 3 | 1 | |
| CO3 | 3 | 3 | 1 | | | | | | 2 | | | 3 | 3 | 1 | |
| CO4 | 3 | 2 | 2 | 2 | | | | | 2 | | | 3 | 3 | 1 | |
| CO5 | 3 | 3 | 3 | 2 | | | | | 2 | | | 3 | 3 | 1 | |
| CO6 | 3 | 3 | 3 | 3 | | | | | 2 | | | 3 | 3 | 2 | |

**Last updated 1st December 2020**