ECE4121: Design for Testability

Programme: B.Tech. (ECE) Year: 4th Yr Semester : 1st Semester
Course : Program Elective (ECE, CCE) Credits : 4/3 Hours : 40 Hrs

Course Context and Overview (100 words):

Overview of digital systems testing and testable design. Test economics, fault modeling, logic and fault simulation, testability measures, test generation for combinational circuits, memory test, delay test, IDDQ test, scan design, and boundary scan.

Prerequisites Courses: Digital VLSI Circuits, Digital System Design

Course outcomes(COs):

On completion of this course, the students will have the ability to:	
CO1:	Understand the economics of testable design and the concept of yield.
CO2:	Learn about defects, errors and faults and their models.
CO3:	Learn about logic and fault simulation: compiled-code and event-driven simulation.
CO4:	Learn about combinational circuit test generation, Memory test, delay test and IDDQ test.
CO5:	Learn about Digital DFT and scan design.

Course Topics:

Topics	Lecture Hours	
UNIT - I **1. Introduction to Testing**	10	
1.1 Introduction, VLSI Testing Process and Test Equipment	3	10
1.2 Test Economics and Product Quality	3	
1.3 Fault Modeling	4	
UNIT - II **2. Test Methods**	20	20
2.1 Logic and fault simulation	6	
2.2 Diagnosis ,Testability measures	4	
2.3 Combinational circuit Automatic Test Pattern Generation (ATPG), Sequential circuit ATPG	6	

2.4 Memory test and Delay test	2	
2.5 IDDQ test	2	
UNIT - III **3. Design for Test (DFT)**	10	10
3.1 Scan design	3	
3.2 Built-In-Self-Test (BIST)	3	
3.3 Boundary Scan Standard	2	
3.4 System test and core-based design	2	

Textbook references (IEEE format):
Text Book:

[1]. Bushnell and V. Agrawal, *"Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits"*, Kluwer Academic Publishers, 2000

Reference books:

[1]. M. Abramovici, M. Breuer, and A. Friedman, *"Digital Systems Testing and Testable Design,* IEEE Press, 1990
[2]. J. Van De Goor, *"Testing Semiconductor Memories: Theory and Practice"*, Wiley and Sons, 1991
[3]. Krstic and K. Cheng, *"Delay Fault Testing for VLSI Circuits",* Kluwer Academic Publishers, 1998
[4]. Stroud, *"A Designer's Guide to Built-in Self-Test",* Kluwer Academic Publishers, 2002

Additional Resources (NPTEL, MIT Video Lectures, Web resources etc.):

Evaluation Methods: Evaluation criteria will be shared by the concerned course instructor.

Prepared By:
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