The LNMIIT, Jaipur Department of Electronics and Communication Engineering Introduction to VLSI (ECE-224)	LNMIIT The LNM Institute of Information Technology

Programme: B. Tech. (ECE)	Course Title: Introduction to VLSI			Course Code: ECE224
Type of Course: Program Core	Prerequisites: Analog Electronics and Basic Electronics			Total Contact Hours: 40
Year/Semester: 2/Even	Lecture Hrs/Week: 3	Tutorial Hrs/Week: 0	Practical Hrs/Week: 0	Credits: 3

Learning Objective:

This course is to teach thorough understanding of the Digital VLSI circuits using MOSFET, design, application, and technology of integrated circuits and systems. To teach MOS transistor models, CMOS logic families including static, dynamic and dual rail logic. Integrated Circuit Layout: Design Rules, Parasitic elements. It covers building blocks like ALU's, FIFO's, counters, memories etc. It also includes VLSI system design with various methodologies like data and control path design, practical design aspects like floor-planning, interconnect issues and various hazards.

Course outcomes (COs):

On completion of this course, the students will have the ability to:		Bloom's Level
CO-1	To **define** and **understand** the key concepts of MOSFETs in Digital VLSI circuit design, theory and implementation	**1, 2**
CO-2	To **explain** and **analyze** the MOS device/circuits working, characteristics and **implement** in digital logic	**2, 3, 4**
CO-3	To **demonstrate** and **examine** the analog circuits and layout using IC design tools like cadence, spice etc	**3, 4**
CO-4	To **list** and **analyze** the various second/ third order effects, practical limitations and non-linearity associated with the technology	**1, 4**
CO-5	To **identify** and **understand** the layout, **apply** the specific design methodology in the suitable circuit to achieve desire outcome	**1, 2, 3**
CO-6	Explain the role of the MOS family in VLSIC domain by offering the very high level of the integration in current technologies	**2**

Course Topics	Lecture Hours	
UNIT – I (MOS Transistor)	**8**	**8**
1.1 Introduction, MOS Transistor Basics and Theory.	**2**	
1.2 Threshold voltage, MOSFET I-V and C-V characteristics, capacitive elements of MOS devices..	**4**	
1.3 Logic implementation by CMOS	**2**	
UNIT – II (MOS INVERTERS: STATIC CHARACTERSTICS)	**8**	**8**
2.1 Static CMOS invertor and its Transfer characteristics	**3**	
2.2 Transistor sizing, Technology scaling, Gate delay	**3**	
2.3 Static characteristics, Noise margins	**2**	

UNIT – III (MOS INVERTERS: SWITCHING CHARACTERISTICS AND INTERCONNECT EFFECTS)	**7**	**7**
3.1. Logical effort, Electrical effort, intrinsic/extrinsic delay	**2**	
3.2. Circuit topologies and transistor sizing for optimal delay and power.	**2**	
3.3. Circuit Styles: Static CMOS circuits, Pass transistor logic, Transmission gate, Dynamic CMOS characterstics, Dual-rail-domino logic, Pseudo MOS logic and other families.	**3**	
UNIT-IV (COMBINATIONAL AND SEQUENTIAL MOS LOGIC CIRCUITS)	**10**	**10**
4.1 Combination circuit design with various architectures	**3**	
4.2 Sequential circuit design, Basic understanding, design and timing analysis of sequential circuits like Flip- Flops and Latches	**4**	
4.3 Timing and pipelining, Clocking techniques, Stick diagram and Layout design	**3**	
UNIT-V (Semiconductor Memories and Low power CMOS Logic Circuits)	**7**	**7**
5.1 Memory design, Read-Only Memory(ROM) Circuits, EEPROM, DRAM, SRAM.	**4**	
5.2 IOs, Low Power Techniques, Design methods and tools, CMOS testing, System Design Examples	**3**	

Textbook References:

Text Book:

1. J. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall India, 1997.
2. Sung-Mo (Steve) Kang and Yusuf Leblebici: CMOS Digital Integrated Circuits Analysis & Design, TATA McGraw Hill Education, 2002.
3. Douglas A. Pucknell and Kamran Eshraghian: Basic VLSI design, Prentice-Hall of India Pvt. Ltd, 1994.

Reference books:

- N. Weste and David Harris, Principles of CMOS VLSI Design, Addison Wesley. 2004.
- L. Glaser and D. Dobberpuhl, The Design and Analysis of VLSI Circuits, Addison Wesley, 1985.
- Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & Sons, 2002.

Additional Resources:

http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
http://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-374-analysis-and-designof-digital-integrated-circuits-fall-2003/lecture-notes/
http://iiscs.wssu.edu/drupal/taxonomy/term/3119

Evaluation Method	
Item	**Weightage (%)**
Quizzes	25

Midterm	25
Final Examination	50

*Please note, as per the existing institute's attendance policy the student should have a minimum of 75% attendance. Students who fail to attend a minimum of 75% lectures will be debarred from the End Term/Final/Comprehensive examination.

CO and PO Correlation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	1									3	3	1	
CO2	3	3	2									3	3	1	
CO3	3	3	2	1								3	3	1	
CO4	3	2	1									3	3	1	
CO5	3	3	3	2								3	3	1	
CO6	3	3	3	1								3	3	2	1

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Updated By:

Approved By: