CSE111 : Digital Systems

Programme: B.Tech (CSE)	Year: 1	Semester: 2
Course: Program Core	Credits: 3	Hours: 40

Course Context and Overview:
This course is designed especially for computer science students, to provide them an introduction of various components involved in specification and implementation of digitals systems. Students will learn to design code to validate their design for various digital modules. They will also learn the details about the design of basic components of a computer. On the completion of this course student will be able to design, analyze, and evaluate digital Systems.

Prerequisites Courses: NIL

Course outcomes (COs):

On completion of this course, the students will:	
CO1**:**	Understand number representation, conversion between different representations, and arithmetic for digital systems.
CO2**:**	Analyze and implement logical operations using combinational system combinational module including ALU.
CO3**:**	Understand, analyze and implementation of sequential system and sequential module.
CO4**:**	Design digital system using RTL
CO5:	Implementation of digital systems using descriptive language and programmable modules.

Course Topics:

Contents	Lecture Hours
UNIT 1 Introduction	7
Introduction, importance, application and type of digital Systems, digital Systems Specification and implementation, analysis and design	
Data Representation and Number System: Number representation, various Binary Codes, Floating Point representation, Signed and Unsigned Numbers, Arithmetic operations including floating point	
UNIT 2 Combinational Systems	2
Introduction: Specification Combinational systems, High-level specification of combinational systems, Binary specification of combinational systems: Boolean functions, Boolean expressions.	
Combinational Circuits: gates, universal set, physical specification: Propagation delays, transition times and effect of load, Voltage variations and noise margins, Power dissipation and delay-power product.	2

Combinational Network Design: Description and characteristics of gate networks, Analysis of gate networks, Minimal two-level networks, Karnaugh maps, Minimization of sum of products and product of sums, Design of multiple-output two-level gate networks, Two-level NAND-NAND and NOR-NOR networks, Networks with XOR and XNOR gates, Networks with 2-input multiplexers.	5
UNIT 3 Combinational Modules	
Standard Combinational Modules: Decoders, Encoders, Priority encoders, Multiplexers, De-multiplexers, Shifters, network design using modules.	4
Arithmetic Combinational Modules: ALU modules and networks (Adder, Substractor, Multiplier, Divisor, Comparator modules)	3
UNIT 4 Sequential System	
Sequential Network Design: High-level and binary implementations, Gated-latch and D flip-flop, Timing characteristics of sequential networks, Analysis of sequential networks, Design of sequential networks, Other flip-flop modules: SR, JK, T; Analysis of networks with flip-flops, Design of networks with flip-flops, Design using state assignments: One-flip-flop-per-state, Shifting state register.	5
Standard Sequential Modules: Registers, Shift registers, Counters, Multi-module systems.	3
Unit 5 RTL System design	
RTL System design: Organization of systems (functional and control unit), RTL System organization, ASM chart, Digital system design using ASM chart: **Data and Control Subsystems:** Data subsystem (Storage modules, Register file, Random-access memory, Functional modules, Datapaths), Control Subsystem.	5
UNIT 6 Implementation of Digital System	
Verilog HDL: Introduction to Verilog, Implementation of complex digital system. (Multiplier/ Divider/ Sort/ Traffic light controller etc.)	4
Programmable Modules: PAL, PLA, PSA, CPLD, and FPGAs. Read-only memories (ROM).	

Textbook:

1. Ercegovac M., Lang T. & Moreno J. H., "*Introduction to Digital Systems"*, John Wiley, 2009.
2. Brown S. and Vranesic Z., "*Fundamentals of Digital Logic with Verilog Design",* Edition 2nd, McGraw-Hill, Inc., New York, NY, USA, 2007.
3. Mano M. M. and Ciletti M. D., "*Digital Design",* Edition 4th. Prentice-Hall, Inc., Upper Saddle River, NJ, USA, 2006.

Evaluation Methods:

Item	Weightage
Quiz/Assignment/Project	35
Midterm	20
Final Examination	45

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